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University of Jordan
Computer Engineering Department
CPE439
Computer Design Lab

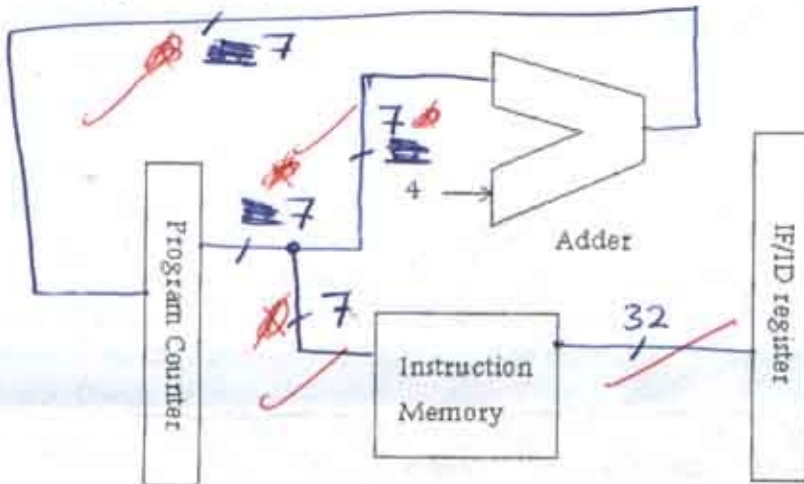
Name: _____
Reg. No. _____

Date: April, 13 2005

Midterm Exam

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Q1. For the figure below,



Assuming the Instruction memory consists of 32×4 bytes
 \downarrow \downarrow
 5 bits 2 bits
 \Rightarrow 7 bits

~~Assume Instruction memory on processor~~ Fetch stage

- 1 (1) What is the name of this stage? Instruction
- 4 (2) Draw the necessary connections to complete the diagram. Show the size of each connection (in bits) as you used them in the lab experiment.
- 2 (3) Using behavioral modeling, write a Verilog module that describes the Adder module above. (Assume addition delay = 12 units).

```

module Adder ( Result, In1, In2 ) ;
    input [6:0] In1, In2 ;
    output [6:0] Result ;
    reg [6:0] Result ;
    always @ ( In1 or In2 ) Begin
        # 12 ;
        Result = ( In1 + In2 ) ;
    end
endmodule
    
```

zero

(4) If the instruction memory access time is 8 units, and each of the two registers (the PC and IF/ID) requires 2 units of propagation delay, what is the minimum clock cycle time required for this stage to operate properly? Explain your answer.

Minimum Clock For this stage $[PC \text{ time} + IM \text{ time}] = 2 + 8 = 10$ units
 because ~~at~~ at the clock edge the new PC address requires 2 units of propagation delay while the IM requires 8 units then the new instruction will be waiting to be stored in the IF/ID register at the new clock edge.

(4) Q2. The following is a sequence of instructions to be performed by the 5-stage pipeline developed in Experiment 3.

- lw R1, 12(R0)
- lw R2, 16(R0)
- lw R3, 20(R0)
- lw R4, 24(R0)
- or R5, R1, R1
- slt R6, R1, R2
- add R7, R1, R2

extra EX/MEM
 F I D I E M I W B

1010
 11
 1100

Assume all registers in the register file are initialized to zeros, all memory word locations in the data memory are initialized to the value "3", and the first instruction is fetched at Cycle 1.

2 (1) A monitoring circuit is added to the design to watch the value that corresponds to the ALU result at the output of the EX/MEM register. What should the monitored value be for each of the following cycles?

Cycle	1	2	3	4	5	6	7	8	9	10
Value (in hexadecimal)	X	X	C	10	14	18	30	0	6	X

2 (2) A monitor circuit is added at the output of the Control Unit to watch the signals: MemRead, RegWrite and ALUSrc. What should the monitored value be for each of the following cycles?

ALUSrc	Operation
0	Select From the Register File
1	Select from the Sign Extend Unit

Cycle	1	2	3	4	5	6	7	8	9	10
MemRead	X	1	1	1	1	X	X	X	X	X
RegWrite	X	1	1	1	1	1	1	1	0	0
ALUSrc	X	1	1	1	1	0	0	0	X	X

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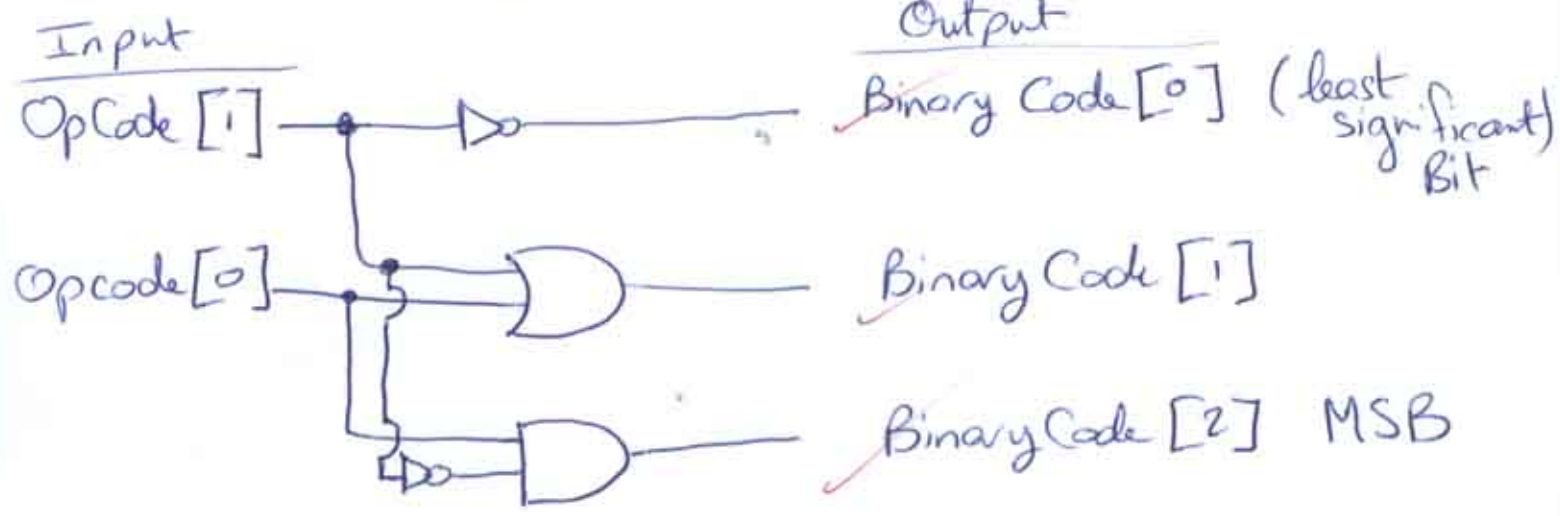
Q3. Design a Control Unit that takes as an input the opcode of an instruction, and generates the corresponding three bits that tell the ALU what operation to perform on the specified operands. Show a complete design and implement it using verilog structural modeling. You can use the basic gates available in Lib439.v
The following data may be used in the design:

Instruction	Opcode
Lw	100011
Or	000000
Slt	000001
Add	000010

ALU Operation	Binary Code
Add	010
Or	001
Slt	111

OpCode 543210 100011	lw →	Add	B.C 210 010
000000	or →	or	001
000001	slt →	slt	111
000010	add →	add	010

opCode → CU



↗
Module
on other
page

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```
Module Controlunit (BinaryCode, OpCode);
```

```
Input, OpCode;
```

```
Input [5:0] OpCode;
```

```
Output [2:0] BinaryCode;
```

```
Wire w1;
```

```
INV I1(BinaryCode[0], OpCode[1]);
```

```
OR or1(BinaryCode[1], OpCode[1], OpCode[0]);
```

```
INV I2(w1, OpCode[1]);
```

```
AND A1(BinaryCode[2], w1, OpCode[0]);
```

```
endmodule
```