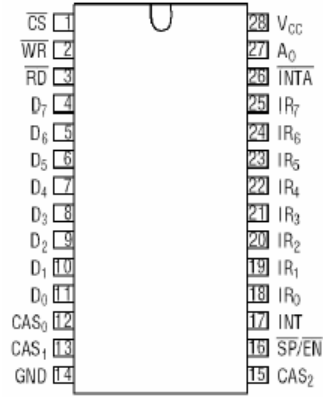


Hardware Interrupts

The 8259A Programmable Interrupt Controller:

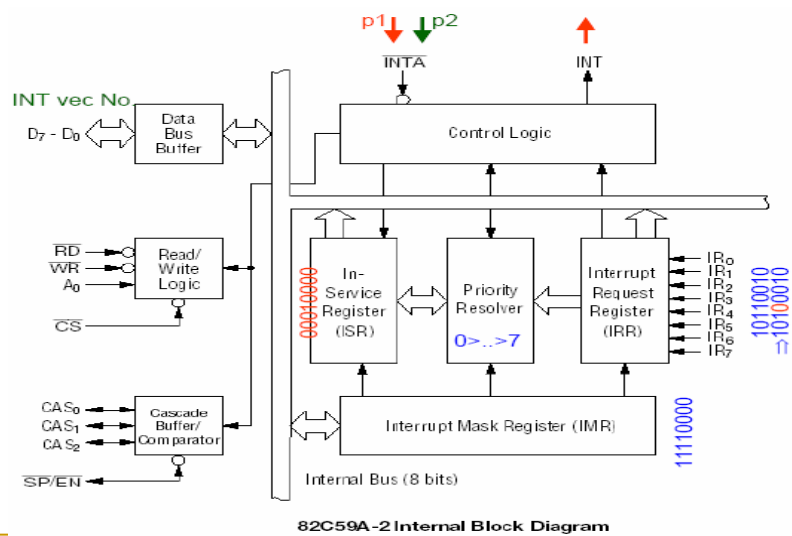
The 8259A Programmable Interrupt Controller (PIC) can handle 8 vector priority encoded interrupts for the microprocessors.



28-pin Plastic DIP

Slide 1

The 8259A Programmable Interrupt Controller:



82C59A-2 Internal Block Diagram

Slide 2

The 8259A PIC

- The **IRR** is an 8-bit register that indicates which interrupt request inputs are active.
- The **ISR** is an 8-bit register that contains the level of the interrupt being serviced.
- The **IMR** is an 8-bit register that holds the interrupt mask bits and indicates which interrupts are masked off.
- The **priority resolver** determines the priorities of the coming interrupt requests and selects the one with the highest priority.

Slide 3

Interrupt Sequence of the 8259A PIC

1. One or more of the interrupt request lines are raised high, setting the corresponding IRR bit(s).
2. The 8259A evaluates these requests and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an \overline{INTA} pulse.
4. Upon receiving an \overline{INTA} from the CPU, the highest priority ISR bit is set and the corresponding IRR bit is reset.

Slide 4

Interrupt Sequence of the 8259A PIC

5. The 8086 will initiate a **second $\overline{\text{INTA}}$ pulse**. During this pulse, the 8259A releases an 8-bit **interrupt vector**, which was partially set with ICW2, onto the data bus where it is read by the CPU.
6. This completes the interrupt cycle. **In the AEOI mode** (AEOI bit of the ICW4 was set) the **ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse**. Otherwise, the ISR bit remains set until an **appropriate EOI command is issued** at the end of the interrupt service routine.

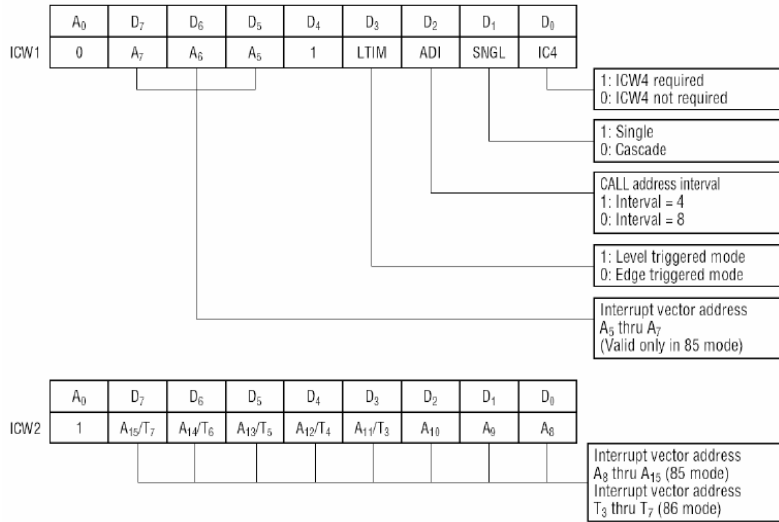
Slide 5

Programming the 8259A PIC

- The 8259A is programmed by initialization and operation command words.
- The **Initialization command words (ICWs)** are programmed before the 8259A is able to function in the system and dictate the basic operation of the 8259A.

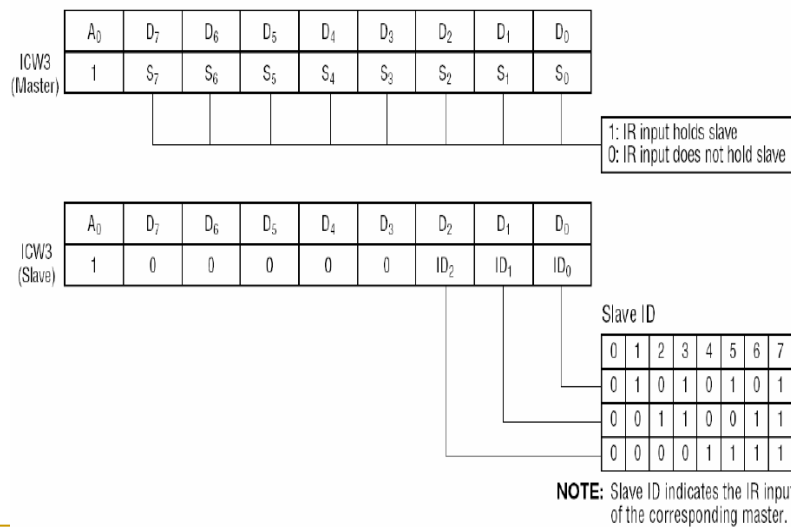
Slide 6

The Initialization Command Words (ICWs)



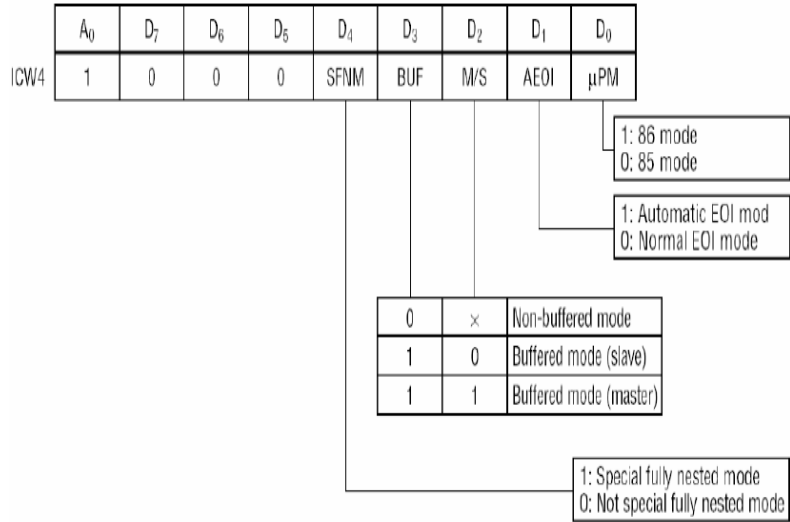
Slide 7

The Initialization Command Words (ICWs)



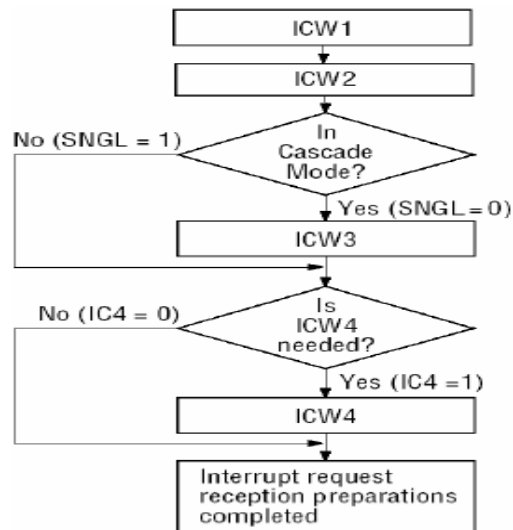
Slide 8

The Initialization Command Words (ICWs)



Slide 9

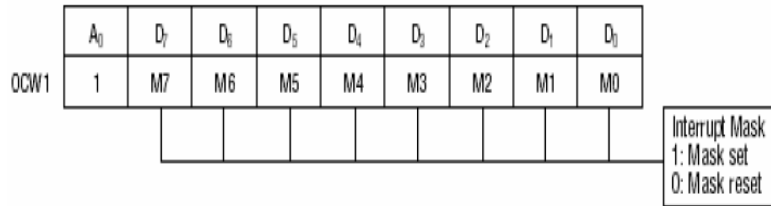
Initialization Sequence



Slide 10

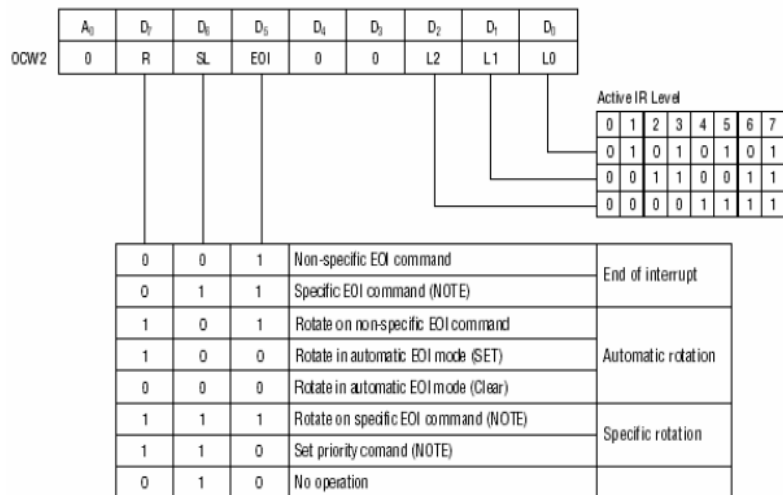
The Operation Command Words (OCWs)

The OCWs are used to direct the operation of the 8259A once it is programmed with the ICW.



Slide 11

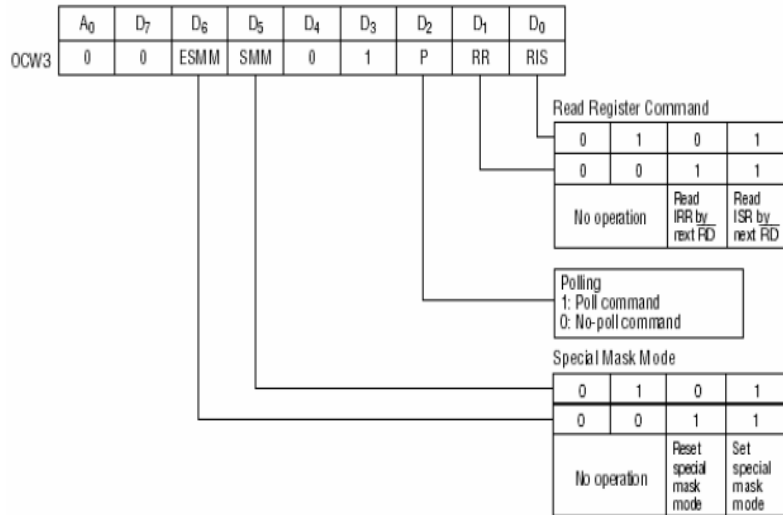
The Operation Command Words (OCWs)



NOTE: L0 thru L2 used

Slide 12

The Operation Command Words (OCWs)



Slide 13

Reading the 8259A Status

- Read 8259A when A0=0 after issuing an OCW3 to get the status of IRR and ISR.

P	RR	RIS	Action
0	1	0	Read IRR
0	1	1	Read ISR

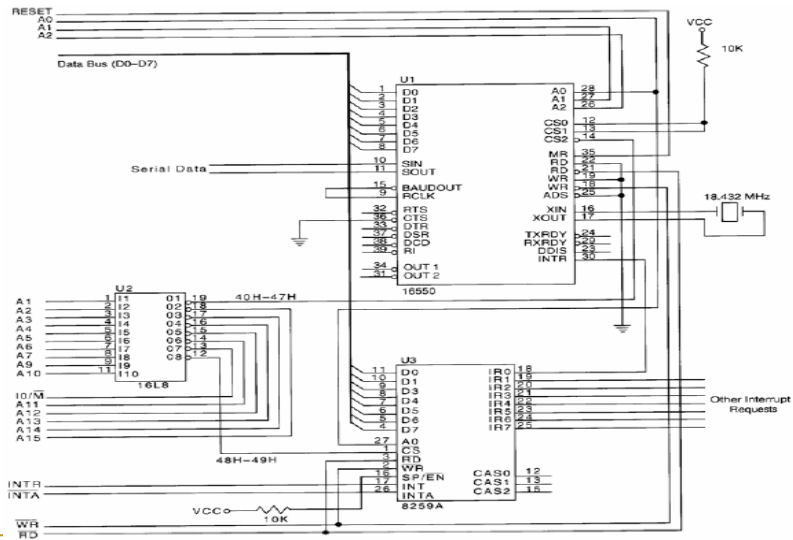
Example: Read IRR (Assume 8259A's port number = 80H)

```
OUT    80H,00001010b
IN     AL,80H
```

- Read 8259A when A0=1 to get the status of IMR.

Slide 14

Interfacing the 16550 UART to the 8088 MP through the PIC 8259A



Slide 15

Interfacing the 16550 UART to the 8088 MP through the PIC 8259A

- An INTR occurs whenever:
 - (1) the transmitter is ready to send another character,
 - (2) the receiver has received a character,
 - (3) an error is detected while receiving data, and
 - (4) a modem interrupt occurs.
- 16550 is decoded at I/O ports 40H-47H.
- 8259A is decoded at I/O port 48H and 49H.

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