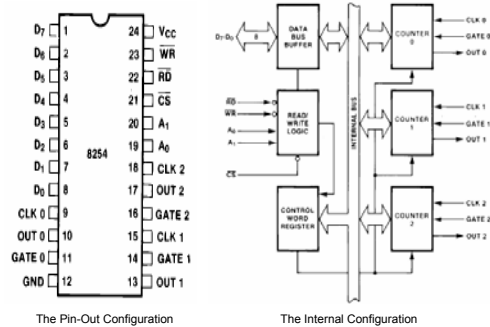


The 8254 Programmable Interval Timer (PIT)

Slide 1

The 8254 PIT



Slide 2

Pin Description

Symbol	Pin No.	Type	Name and Function															
D ₇ -D ₀	1-8	I/O	DATA: Bi-directional three state data bus lines, connected to system data bus.															
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.															
OUT 0	10	O	OUTPUT 0: Output of Counter 0.															
GATE 0	11	I	GATE 0: Gate input of Counter 0.															
GND	12		GROUND: Power supply connection.															
V _{CC}	24		POWER: +5V power supply connection.															
WR	23	I	WRITE CONTROL: This input is low during CPU write operations.															
RD	22	I	READ CONTROL: This input is low during CPU read operations.															
CS	21	I	CHIP SELECT: A low on this input enables the 8254 to respond to RD and WR signals. RD and WR are ignored otherwise.															
A ₁ , A ₀	20-19	I	ADDRESS: Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>A₁</th> <th>A₀</th> <th>Selects</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Counter 0</td> </tr> <tr> <td>0</td> <td>1</td> <td>Counter 1</td> </tr> <tr> <td>1</td> <td>0</td> <td>Counter 2</td> </tr> <tr> <td>1</td> <td>1</td> <td>Control Word Register</td> </tr> </tbody> </table>	A ₁	A ₀	Selects	0	0	Counter 0	0	1	Counter 1	1	0	Counter 2	1	1	Control Word Register
A ₁	A ₀	Selects																
0	0	Counter 0																
0	1	Counter 1																
1	0	Counter 2																
1	1	Control Word Register																
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.															
OUT 2	17	O	OUT 2: Output of Counter 2.															
GATE 2	16	I	GATE 2: Gate input of Counter 2.															
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.															
GATE 1	14	I	GATE 1: Gate input of Counter 1.															
OUT 1	13	O	OUT 1: Output of Counter 1.															

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The Control Word Format

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

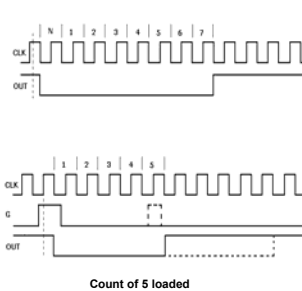
SC—Select Counter		BCD	
SC1	SC0		
0	0		0 Binary Counter 16-bits
0	1		1 Binary Coded Decimal (BCD) Counter (4 Decades)
1	0	Select Counter 2	
1	1	Read-Back Command	

RW—Read/Write		M—Mode			
RW1	RW0	M2	M1	M0	
0	0	0	0	0	Mode 0
0	1	0	0	1	Mode 1
0	1	X	1	0	Mode 2
1	0	X	1	1	Mode 3
1	1	1	0	0	Mode 4
1	1	1	0	1	Mode 5

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Modes of Operation

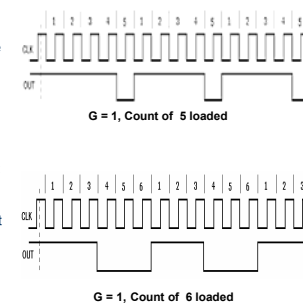
- Mode 0:** Events counter – In this mode, the output becomes a logic 0 when the control word is written and remains there until [N + the number of programmed counts].
- Mode 1:** Re-triggerable, monostable multivibrator (one-shot) – In this mode the G input triggers the counter.



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Modes of Operation

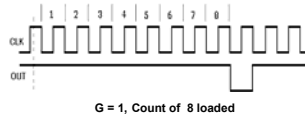
- Mode 2:** Allows the counter to generate a series of continuous pulses that are one clock pulse wide. The separation between pulses is determined by the count.
- Mode 3:** Generates a continuous square wave at the OUT connection, provided that G = 1.
- If the count is even, the output is high for one half of the count and low for one half of the count.
- If the count is odd, the output is high for one clocking period longer than it is low.



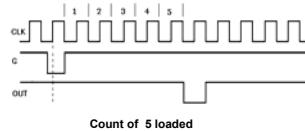
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Modes of Operation

- Mode 4:** Allows the counter to produce a single pulse at the output. If the count is 8, the output is high for 8 clocking periods and low for one clocking period.



- Mode 5:** A hardware triggered one-shot that functions as mode 4, except that it is started by a trigger pulse on the G pin instead of by software.



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The Counter Latch Control Word

- Like a Control Word, this command is written to the Control Word Register, which is selected.

- Like a Control Word, the SC0, SC1 bits select one of the three Counters.

- The two other bits, D5 and D4, distinguish this command from a Control Word.

- If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

$A_1, A_0 = 11; \overline{CS} = 0; \overline{RD} = 1; \overline{WR} = 0$

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5, D4 - 00 designates Counter Latch Command

X - don't care

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

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The Read-back Control Word

- The read-back command may be used to latch multiple counter output latches (OL) by setting the **/COUNT bit D5=0** and selecting the desired counter(s).

- This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed).

- The counter is automatically unlatched when read, but other counters remain latched until they are read.

$A_0, A_1 = 11; \overline{CS} = 0; \overline{RD} = 1; \overline{WR} = 0$

D7	D6	D5	D4	D3	D2	D1	D0
1	1	COUNT	STATUS	CNT 2	CNT 1	CNT 0	0

D5: 0 - Latch count of selected counter(s)
 D5: 1 - Latch status of selected counter(s)
 D3: 1 - Select counter 2
 D2: 1 - Select counter 1
 D1: 1 - Select counter 0
 D0: Reserved for future expansion; must be 0

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The Status Register

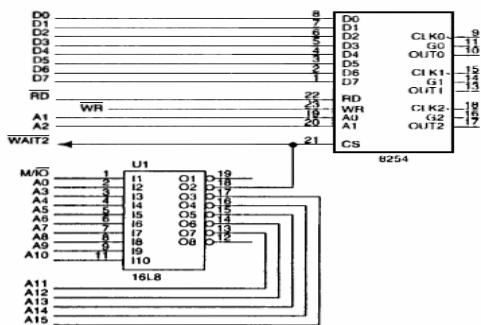
D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D7 1 - Out Pin is 1
 0 - Out Pin is 0
 D6 1 - Null count
 0 - Count available for reading
 D5-D0 Counter Programmed Mode

- The read-back command may also be used to latch status information of selected counter(s) by setting **/STATUS bit D4=0**. Status must be latched to be read; status of a counter is accessed by a read from that counter.

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Timer Interface to Microprocessor



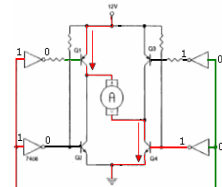
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Application - DC Motor Speed and Direction Control

Motor Operation:

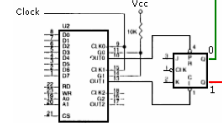
- If the Q output of the J-K flip-flop is a logic-1:

- The transistors: Q1 is off and Q2 is on, with ground applied to the +ve lead of the motor.
- The bases of both Q3 and Q4 transistors are pulled low through the inverters. This causes Q3 to turn on and Q4 to turn off, applying +12V to the -ve lead of the motor.
- This connection causes the motor to spin in one direction.



- If the Q output of the J-K flip-flop is a logic-0:

- The transistors: Q3 is off and Q4 is on, with ground applied to the -ve lead of the motor.
- The bases of both Q1 and Q2 transistors are pulled low through the inverters. This causes Q1 to turn on and Q2 to turn off, applying +12V to the +ve lead of the motor.
- This connection causes the motor to spin in an opposite direction to that of the previous case.

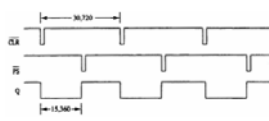


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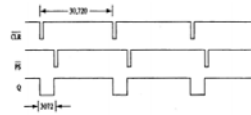
Application - DC Motor Speed and Direction Control

Timing Diagram:

- How each counter generates pulses at different positions to vary the duty cycle at the Q output of the flip-flop? These pulses are also called Pulse-Width Modulation (PWM).
- Both counters operate in mode-2
- No rotation when $t_{on} = t_{off} = 50\%$



- Rotation in reverse direction, $t_{off} = 10\%$

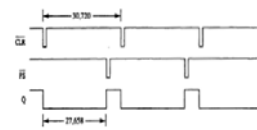


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Application - DC Motor Speed and Direction Control

Timing Diagram:

- Rotation in forward direction, $t_{on} = 90\%$



- To generate these waveforms, counters 0 and 1 are both programmed to divide the input clock (8MHz) by 30,720. The divide rate of 30,720 is divisible by 256, so we can develop a short program that allows 256 different speeds.

- The duty cycle (δ) of Q is varied by changing the point at which counter 1 is started in relationship to counter 0. As this point approaches the starting point of counter 0, the motor increases its speed.

$$\delta\% = (t_{on}/T) \times 100\%$$

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Application Example – Assembly Program

```

;A procedure that controls the speed and direction of the motor
;in Figure 11-40.
;AH determines the speed and direction of the motor where
;AH is between 00H and FFH.
CNTR EQU 706H
CNT0 EQU 700H
CNT1 EQU 702H
COUNT EQU 30720

SPEED PROC NEAR USES BX DX AX
    MOV BL,AH
    MOV AX,120
    MUL BL
    MOV BX,AX
    MOV AX,COUNT
    SUB AX,BX
    MOV BX,AX

    MOV DX,CNTR
    MOV AL,00110100B ;program control words
    OUT DX,AL
    MOV AL,0110100B
    OUT DX,AL

    MOV DX,CNT1
    MOV AX,COUNT
    OUT DX,AL ;to generate a clear
    MOV AL,AH
    OUT DX,AL

    .REPEAT IN AL,DX
            XCHG AL,AH
            IN AL,DX
            XCHG AL,AH
    .UNTIL BX == AX

```

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