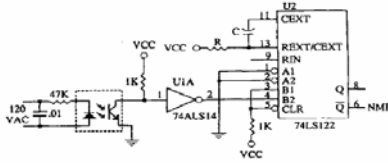


Hardware Interrupts

Non-Maskable Interrupt (NMI):

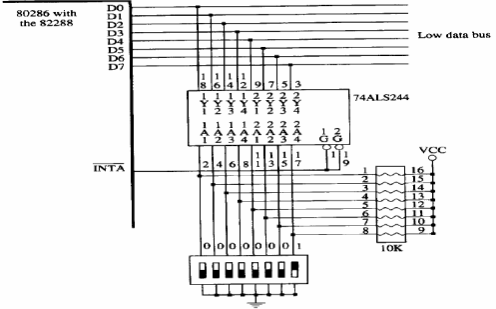
- The NMI is an **edge-triggered** input that requests an interrupt on the positive edge.
- It is often used for **parity errors and other major system faults** such as power failures.



A power failure detection circuit

Slide 1

Applying Interrupt Vector Type Numbers In Response to INTA



A circuit that applies any interrupt vector type number in response to INTA. Here the circuit is applying type number 80H.

Slide 4

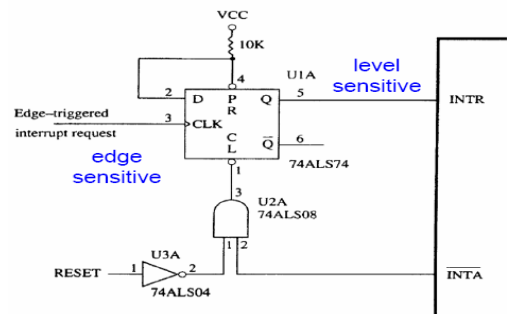
Hardware Interrupts

INTR and INTA:

- INTR is **level-sensitive** and must be held at a logic 1 level until it's recognized.
- The input is **automatically disabled** once it is accepted by the microprocessor (**clear IF**) and **re-enabled** by the IRET instruction (**set IF**) at the end of the interrupt service procedure.
- The microprocessor responds to the INTR input by pulsing the INTA output in anticipation of receiving an interrupt vector number on data bus connection D7-D0.

Slide 2

Turning a Level-sensitive Interrupt to an Edge-sensitive One

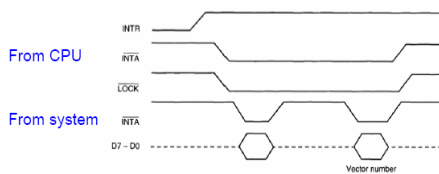


Converting INTR into an edge-triggered interrupt request input

Slide 5

INTR and INTA

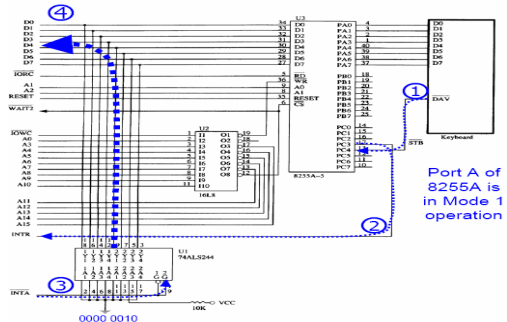
- Two \overline{INTA} pulses will be generated by the system and the content on the data bus will only be interpreted as an **interrupt vector number** during the **second pulse**.



The timing of the INTR input and INTA output. *Note: This portion of the data bus is ignored and usually contains the vector number.

Slide 3

A Keyboard Interface using Interrupt Vector 40H.

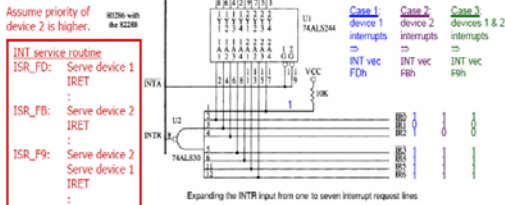


An 8255A-5 interfaced to a keyboard from the microprocessor system using interrupt vector 40H

Slide 6

Expanding the Interrupt Structure

Using the 74ALS244:

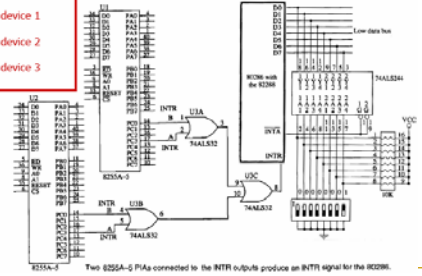


Slide 7

Assume priority: 1>2>3>4

```

INT service routine
ISR_B0:  Check device 1
        JMP Serve_D1 if Yes
        Check device 2
        JMP Serve_D2 if Yes
        Check device 3
        JMP Serve_D3 if Yes
        Serve device 4
        IRET
:
Serve_D1: serve device 1
        IRET
:
Serve_D2: serve device 2
        IRET
:
Serve_D3: serve device 3
        IRET
:
    
```



Slide 10

Expanding the Interrupt Structure

- The 8-input NAND gate will provide a INTR signal when any of the \overline{IR} inputs becomes active.
- Priority must be resolved if more than 1 interrupt request lines become active.
- The **interrupt service procedure** associated with the interrupt vector generated **must resolve the priority of the coming requests** first if more than 1 interrupt request lines become active.

Slide 8

Example of a Daisy-Chain Interrupt Service

EXAMPLE

```

;A procedure that services the daisy-chain interrupt
;
= 0504 C1 EQU 504H ;first 82C55
= 0604 C2 EQU 604H ;second 82C55
= 0001 MASK1 EQU 1 ;INTRB
= 0008 MASK2 EQU 8 ;INTRB

0000 POLL PROC FAR USES AX DX
0002 BA 0504 MOV DX,C1 ;address first 82C55
0005 BC TR AL,DX ;get port C
0006 A9 01 TEST AL,MASK1
0008 75 0F JNZ LEVEL_0 ;if INTRB is set
000A A9 08 TEST AL,MASK2
000C 75 13 JNZ LEVEL_1 ;if INTRB is set
000E BA 0604 MOV DX,C2 ;address second 82C55
0011 BC TR AL,DX ;get port C
0012 A9 01 TEST AL,MASK1
0014 75 1B JNZ LEVEL_2 ;if INTRB is set
0016 KB 29 00 JMP LEVEL_3 ;poll INTRB
0019 POLL ENDP
    
```

Check who generates the INT by reading the status word (port C) of the 8255As. The polling order determines priority.

Slide 11

Expanding the Interrupt Structure

Using Polling Technique:

- Only one interrupt vector is required** for all devices.
- The interrupt service procedure locates which INTR output became active by polling.
- Priority is determined by the order in which the devices issuing requests are polled by the sequence.**

Slide 9